MONOLITHIC KU-BAND GAAS 1-WATT CONSTANT PHASE VARIABLE POWER AMPLIFIER

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ABSTRACT

A GaAs monolithic 1.0 Watt constant phase variable power amplifier has been demonstrated for the first time at Ku-band Compressed gain of this amplifier is greater than 14 dB with >1 Watt output power over the 13.5 to 15 5 GHz band. This amplifier features dual gate FETs which achieve greater than 30 dB of gain control with less than ±10° of phase variation over the entire band.

INTRODUCTION

In an effort to reduce size and cost of transmit/receive, T/R, modules used in airborne phased array radar applications, Monolithic Microwave Integrated Circuits (MMICs) have become a primary focus of many development programs. Integration of MMICs into T/R modules reduces the labor and tuning required by similar hybrid circuits.

Integration of multiple functions on a single monolithic circuit reduces system cost significantly. The constant phase variable-power-amplifier (VPA) described herein combines power amplification and constant phase gain control functions into a single monolithic part. Constant phase VPAs have been demonstrated previously at X-band.[1] However, this is the first report of a 1 Watt constant phase VPA at Ku-band.

Three stages of Dual-Gate FETs (DGFETs) were used to achieve greater than 1-Watt output power with more than 14 dB associated gain under compressed rf drive while providing more than 30 dB of gain control. Minimal phase variation over the gain control range was also desired. Results obtained from related work[1] were used in the selection of the Gate-2 rf termination to minimize phase variations.

FET MODELING

The amplifier consists of three stages of DGFETs. The first, second, and third stages have 800, 3200 and 6400μm gate peripheries, respectively. At the time the amplifier design began existing DGFETs meeting the power and gain requirements of this program were not available in the appropriate device sizes. However, a 450μm DGFET unit cell was identified which met the power and gain requirements. This device is illustrated in Figure 1. Several of these devices were characterized and a DGFET model generated. This model was subsequently scaled to a 800μm unit cell. The 800μm unit cell DGFET model is illustrated in Figure 2

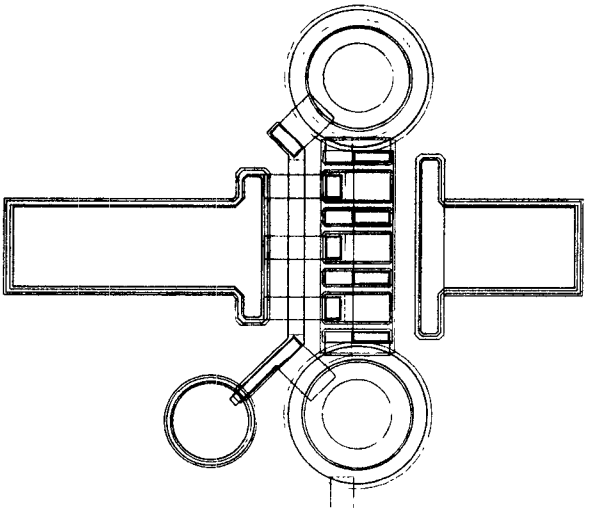

Figure 1. 450μm DGFET Photograph.

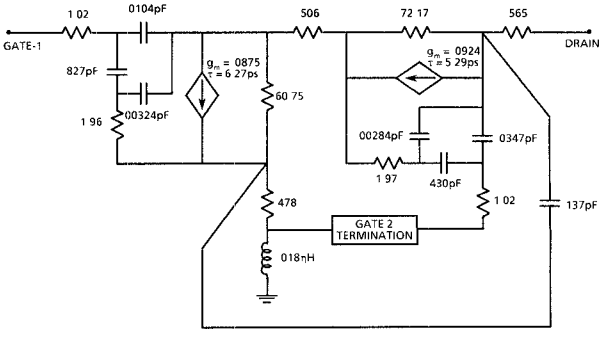

Figure 2. 800μm DGFET Unit Cell Circuit Model.

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The number and configuration of the vias were changed to accommodate compression of the unit cell for multi-cell devices while minimizing the source inductance. In addition, the drain feed air-bridges were curved to provide sufficient space to connect the Gate-2 rf bus to the Gate-2 capacitor top plate located on the newly configured vias. An illustration of the 800μm DGFET unit cell is provided in Figure 3.

The capacitance values were changed to provide series resonance between the via inductance and the capacitor at 14.5 GHz. This in-band resonance has previously been determined[1] as the optimum Gate-2 rf termination for mimimum phase variation over the gain control range. The drain electrode pads beneath the source air-bridges were also notched to reduce drain-to-source coupling, Figure 3.

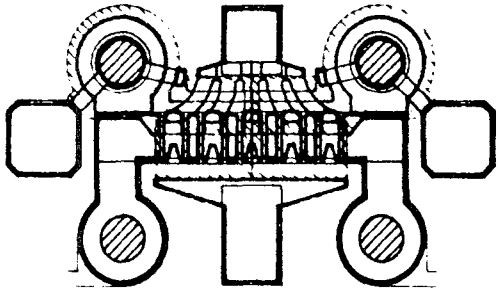

Figure 3. 800μm DGFET Unit Cell Photograph.

The gain compression characteristics of the 450μm DGFET were measured on several devices. The output power 1 dB compression point of the device was plotted as a function of gate periphery on a semi-log graph.

As an estimate of the scaled increase in output power for increased gate width, a factor of 2.7 dB/octave increase in gate periphery was used. This conservative extrapolation is intended to account for increased heat dissipation, increased phase errors and combining losses.

The second and third stage device sizes were chosen by estimating the power required at the output of each stage. The resulting second and third stage gate peripheries were 3200μm and 6400μm.

AMPLIFIER DESIGN

The 800μm unit cell was integrated into both the second stage and third stage devices. Resistive shunt feedback was used around the second stage device. Segmented mesa resistors were used to provide gain programmability without varying the gate biases.

Since feedback was used around the second stage, the device was designed to operate near the linear region. Series resistance was used in the Gate-1 matching circuitry of both the first and second stage devices to ensure stability. The series resistor used in the first stage gate circuitry also improves the input matching characteristic.

In an attempt to minimize chip size the second stage drain bias is injected through a shorted stub connected to the feedback loop. Incorporation of this shorted stub into the feedback loop eliminates an additional shorted stub from the second interstage matching circuitry. An approximate 5% reduction in overall chip length resulted from this alone.

The load-line impedance was determined by load-pull measurements performed at Sandia National Laboratories on the 450μm DGFETs. The resulting impedance loci were scaled from the 450μm device to a 6400μm device. A fifth-order output matching circuit was designed to present the final stage DGFET with the desired load-line impedance.

All gate and drain bias lines were bussed together and routed to the input and output of the amplifier respectively. The overall amplifier dimensions are 0.190 x 0.300 x 0.006 in. A photograph of a packaged 1-Watt constant phase variable power amplifier is provided in Figure 4.

AMPLIFIER PERFORMANCE

The power amplifier performance was measured with a 16 dBm drive level. These amplifiers typically demonstrate >14 dB gain with >15 dB return loss from 13.5 to 15.5 GHz. The gain and return loss of a typical amplifier is illustrated in Figure 5.

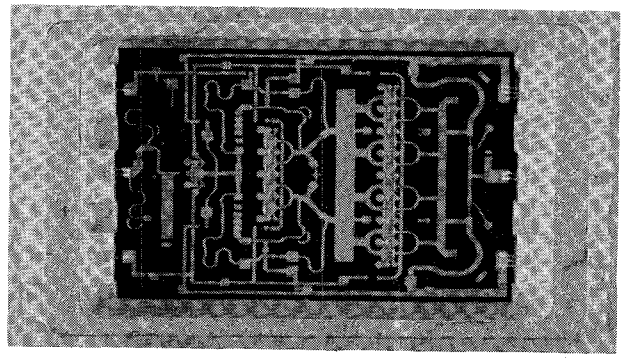

Figure 4. Packaged 1-Watt Variable Power Amplifier.

The data in Figure 5 is at room temperature under CW conditions. The amplifier requires approximately 1.4 Amperes of current with 8 Volts applied to the drain at this rf drive level. The

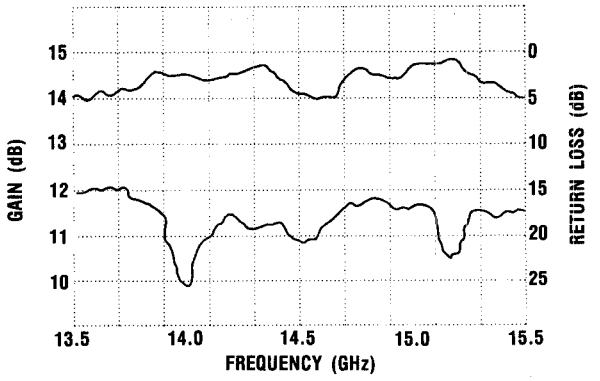

Figure 5. Typical Power Amplifer Gain and Return Loss (P_{in} = 16 dBm).

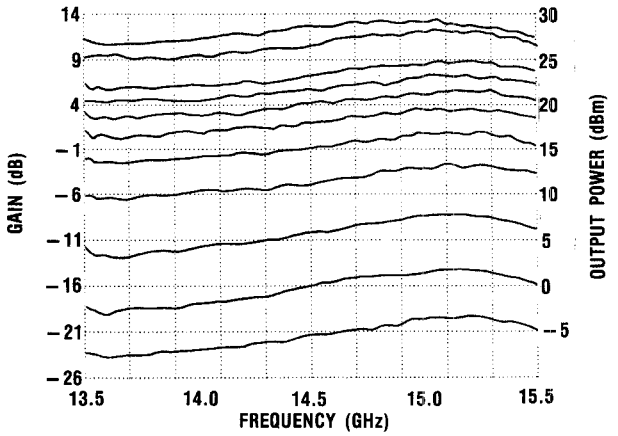

Figure 6. Typical Power Amplifier Gain Control Characteristic.

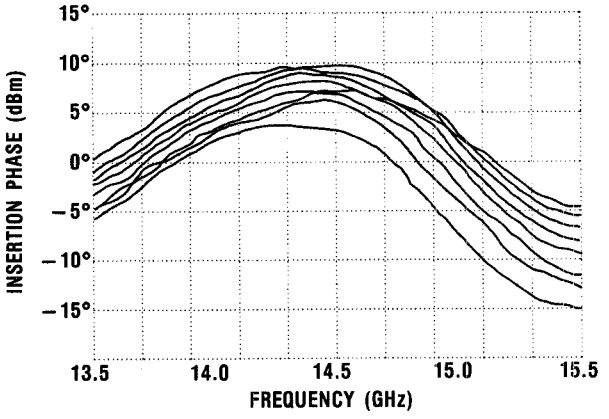

Figure 7. Typical Insertion Phase Variations of the Power Amplifer.

amplifier demonstrates greater than 30 dB of gain control under large signal rf excitation, Figure 6. This gain control is achieved by varying the applied Gate-2 bias potential.

The variations in the transmission phase as a function of gain control are illustrated in Figure 7. The worse case variations occur at 15.5 GHz. However, phase variations remain less than ± 10° across the entire 13.5 to 15.5 GHz band.

SUMMARY

A three stage DGFET constant phase variable power amplifier has demonstrated 14 dB of gain with greater than 1 watt of output power over the 13.5 to 15.5 GHz band. The amplifier has also demonstrated >30 dB of gain control with less than ± 10° of phase variation. The input return loss is typically > 15 dB across the 13.5 to 15.5 GHz Band.

ACKNOWLEDGEMENTS

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REFERENCES

[1] D. M. Drury, D. C. Zimmermann and D. E. Zimmerman, "A Dual-Gate FET Constant Phase Variable Power Amplifier," 1985 IEEE MTT-S International Microwave Symposium Digest.